LISTING OF CLAIMS

1. (Previously Presented) An arbiter in a system, the arbiter comprising:

at least one interface for generating a pseudo-grant signal to all requesting master units at the same time and for receiving transaction information from all requesting master units in response to the pseudo-grant signal.

2. (Previously Presented) The arbiter of claim 1, the arbiter further performing arbitration based on the transaction information received from all the requesting master units.

3. (Previously Presented) The arbiter of claim 1, the at least one interface including a master interface for generating the pseudo-grant signal to all the requesting master units, for receiving the transaction information from all the requesting master units in response to the pseudo-grant signal, and for generating a ready signal to a selected one of the requesting master units.

4. (Original) The arbiter of claim 3, the master interface including at least one generator for generating the pseudo-grant signals from at least one request signal from all the requesting master units.

5. (Original) The arbiter of claim 3, the master interface including at least one circuit for converting a target slave ready signal from at least one slave into a data transfer ready signal for a selected one of the requesting master units.

6. (Original) The arbiter of claim 3, wherein the ready signal is for data transfer.

7. (Original) The arbiter of claim 3, wherein the ready signal indicates bus availability.

8. (Previously Presented) The arbiter of claim 1, the at least one interface including a controller interface for requesting at least one slave unit to prepare for data transfer in response to the target information from the selected one of the requesting master units.

9. (Original) The arbiter of claim 8, wherein the controller interface is a slave controller interface which interacts with at least one slave controller of the at least one slave unit.

10. (Original) The arbiter of claim 9, wherein each slave controller controls at least one slave memory.

11. (Original) The arbiter of claim 8, wherein the controller interface is an SDRAM controller interface which interacts with at least one SDRAM controller of the at least one slave unit.

12. (Original) The arbiter of claim 11, wherein each SDRAM controller controls at least one SDRAM memory bank.

13. (Original) The arbiter of claim 1, wherein a request from all the requesting master units is synchronized with a system clock.

14. (Previously Presented) A system comprising:

at least two master units for generating a request;

an arbiter for receiving the request from the at least two master units and for generating a pseudo-grant signal at the same time in response to the request from the at least two master units;

the at least two master units supplying target information to the arbiter in response to the pseudo-grant signal; and

at least one slave unit preparing for data transfer in response to the target information supplied by the at least two master units.

15. (Previously Presented) The system of claim 14, wherein the at least one slave unit completes preparing for data transfer and data is transferred between one of the at least two master units and one of the at least one slave units.

16. (Original) The system of claim 14, wherein all requesting master units in the system receive the pseudo-grant signal from the arbiter.

17. (Previously Presented) The system of claim 14, wherein the request from the at least two master units is synchronized with a system clock.

18. (Previously Presented) The system of claim 14, wherein the pseudo-grant signal from the arbiter and the target information from the at least two master units are synchronized.

19. (Previously Presented) A method of performing arbitration in a system, comprising:
generating a pseudo-grant signal, in response to at least two requests, at the same time, and
receiving target information in response to the pseudo-grant signal.

20. (Original) The method of claim 19, further comprising:
performing arbitration based on the target information.

21. (Previously Presented) The method of claim 19, wherein the at least two requests and the target information are from a plurality of master units.

22. (Original) The method of claim 19, wherein the pseudo-grant is generated in response to all requests.

23. (Original) The method of claim 19, further comprising:
requesting preparation for data transfer in response to the target information.

24. (Original) The method of claim 19, wherein the request is synchronized with a system clock.

25. (Original) The method of claim 19, wherein the method is software or hardware implemented.

26. (Previously Presented) A method of performing arbitration in a system, comprising:
generating at least two requests;

receiving the at least two requests and generating a pseudo-grant signal in response to the at least two requests at the same time;

supplying target information in response to the pseudo-grant signal; and

preparing for data transfer in response to the target information.

27. (Previously Presented) The method of claim 26, wherein the at least two requests and the target information are from a plurality of requesting master units.

28. (Original) The method of claim 27, further comprising:

completing preparation of data transfer; and

transferring data.

29. (Previously Presented) The method of claim 28, wherein said generating, receiving, supplying, and preparing constitute a first stage and said completing and transferring constitute a second stage and said first and second stages occur concurrently.

30. (Original) The method of claim 29, wherein completing preparation of data transfer includes determining whether a bus is available and selecting one of the requesting masters.

31. (Original) The method of claim 26, wherein the pseudo-grant signal is generated in response to all requests.

32. (Original) The method of claim 26, wherein the request is synchronized with a system clock.

33. (Original) The method of claim 26, wherein the method is software or hardware implemented.